

FIGURE 1 (Prior Art)

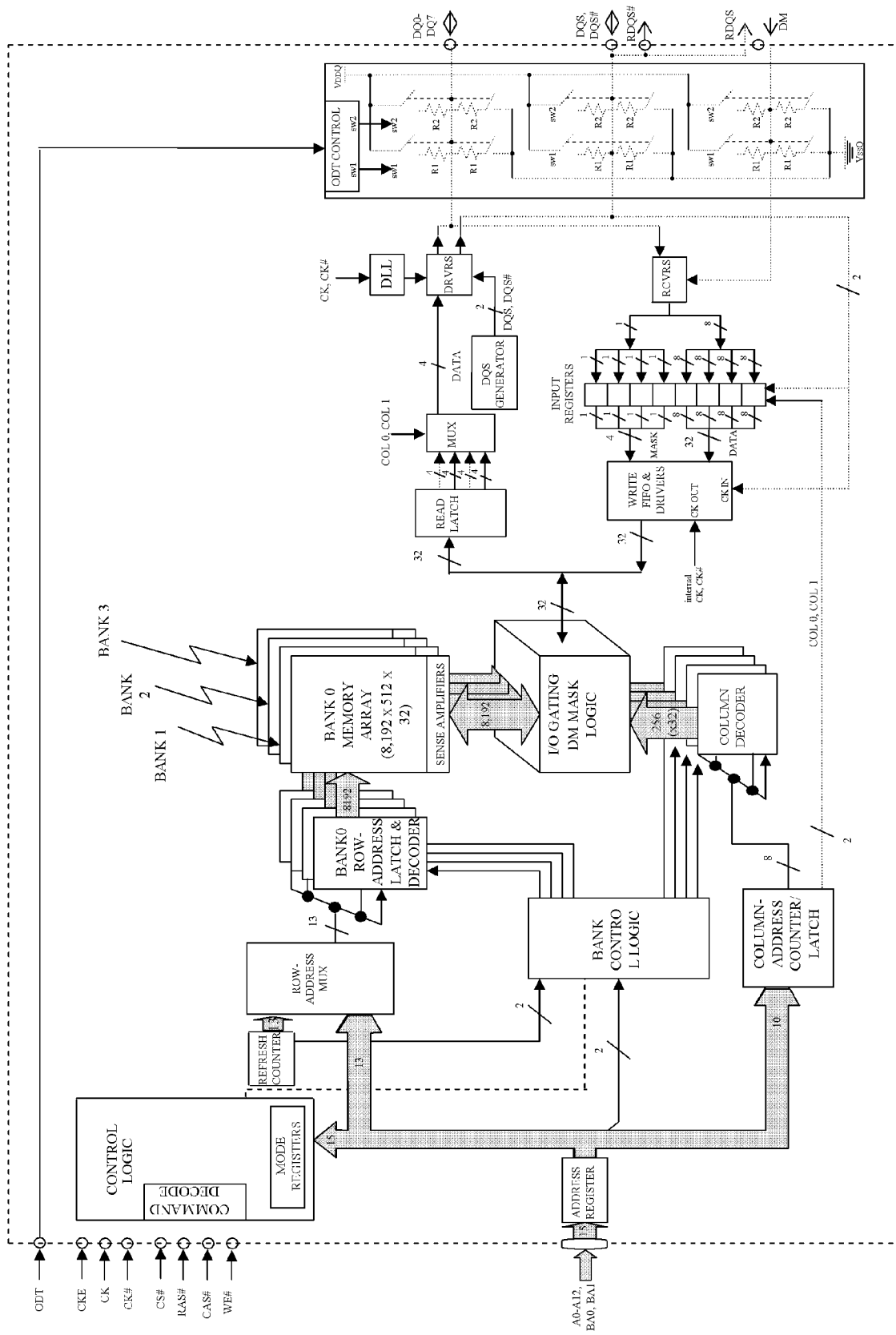


FIGURE 3 (Prior Art)

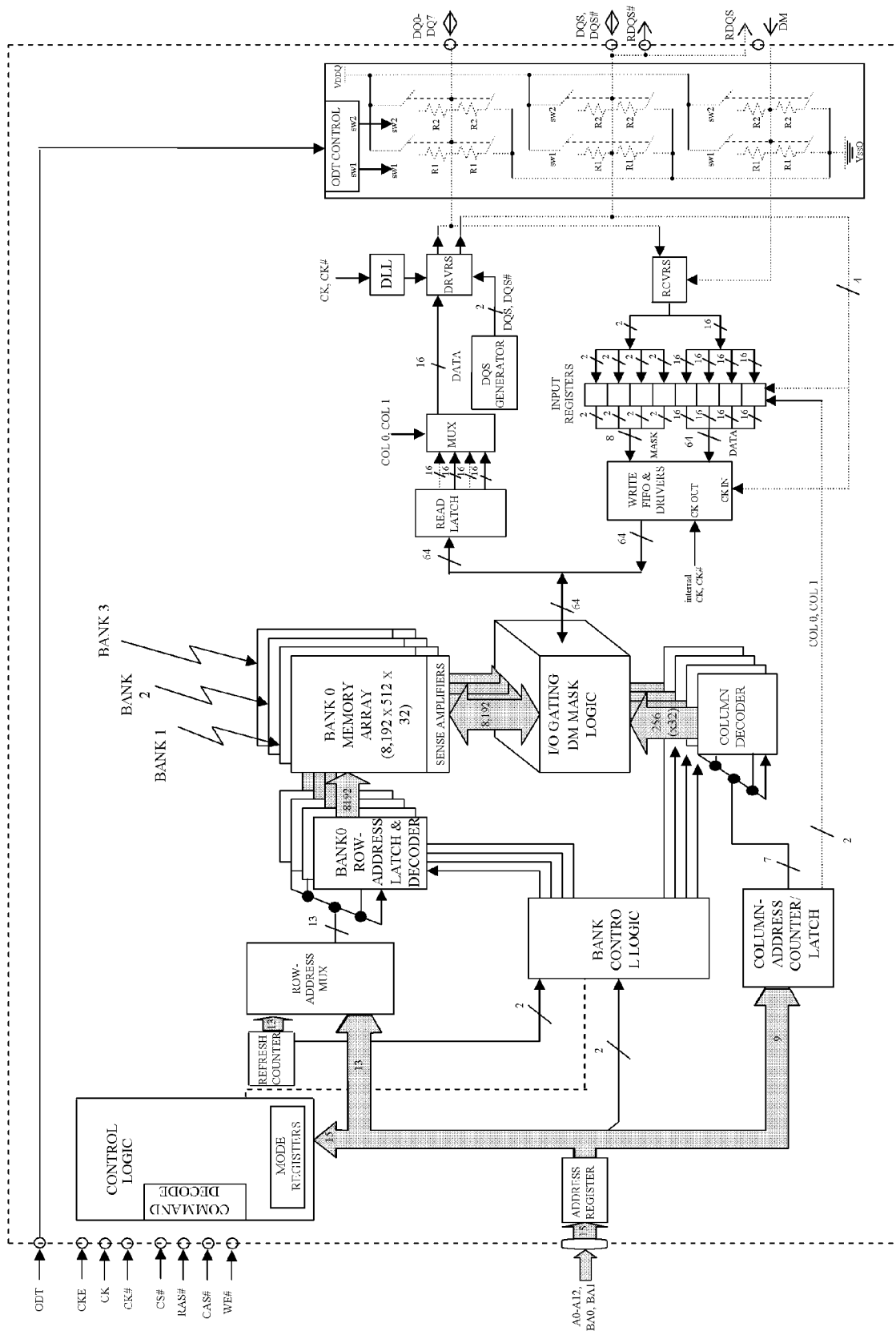
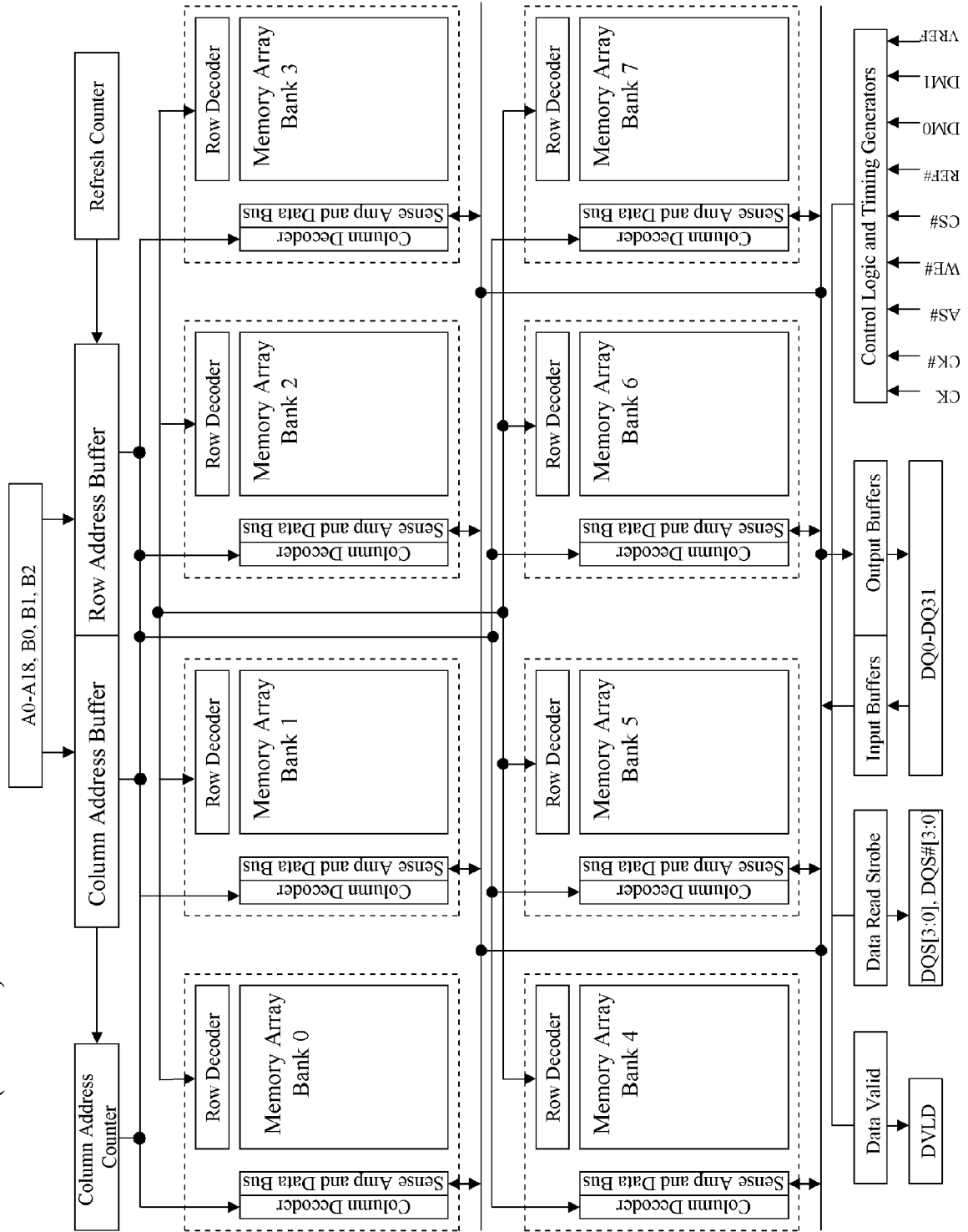


FIGURE 4
(Prior Art)



The diagram illustrates a memory architecture with eight memory banks (Bank 0 to Bank 7). Each bank contains a Memory Array, a Row Decoder, a Column Decoder, and Sense Amps and Data Buses. The memory array is connected to a Refresh Counter, a Column Address Buffer, and a Row Address Buffer. The Column Address Buffer is connected to a Column Address Counter. The Row Address Buffer is connected to a Row Address Counter. The memory array is also connected to a Control Logic and Timing Generator, which provides signals for VREF, DM, REF#, CS#, WE#, DR#, DQ#, and CR. The memory array is connected to Input Buffers and Output Buffers, which are connected to the DQ0-DQ35 data bus. The memory array is also connected to an Output Data Valid signal and a QVLD signal.

The diagram illustrates a memory architecture with eight memory banks (Bank 0 to Bank 7). Each bank contains a Memory Array, a Row Decoder, a Column Decoder, and Sense Amps and Data Buses. The architecture is controlled by a Refresh Counter, Column Address Buffer, Row Address Buffer, and Control Logic and Timing Generator. The Control Logic and Timing Generator provides signals for CK, CK#, DK, DK#, WE#, CS#, REF, DM, and VREF. The memory array is connected to Input Buffers (DO - D17) and Output Buffers (Q0 - Q17). The Column Address Buffer and Row Address Buffer are connected to the Column and Row Decoders, respectively. The Refresh Counter is connected to the Row Address Buffer. The Control Logic and Timing Generator is connected to the Column Address Buffer, Row Address Buffer, and the memory array. The memory array is connected to the Input Buffers and Output Buffers. The Column Address Buffer and Row Address Buffer are connected to the Column and Row Decoders, respectively. The Refresh Counter is connected to the Row Address Buffer. The Control Logic and Timing Generator is connected to the Column Address Buffer, Row Address Buffer, and the memory array. The memory array is connected to the Input Buffers and Output Buffers.

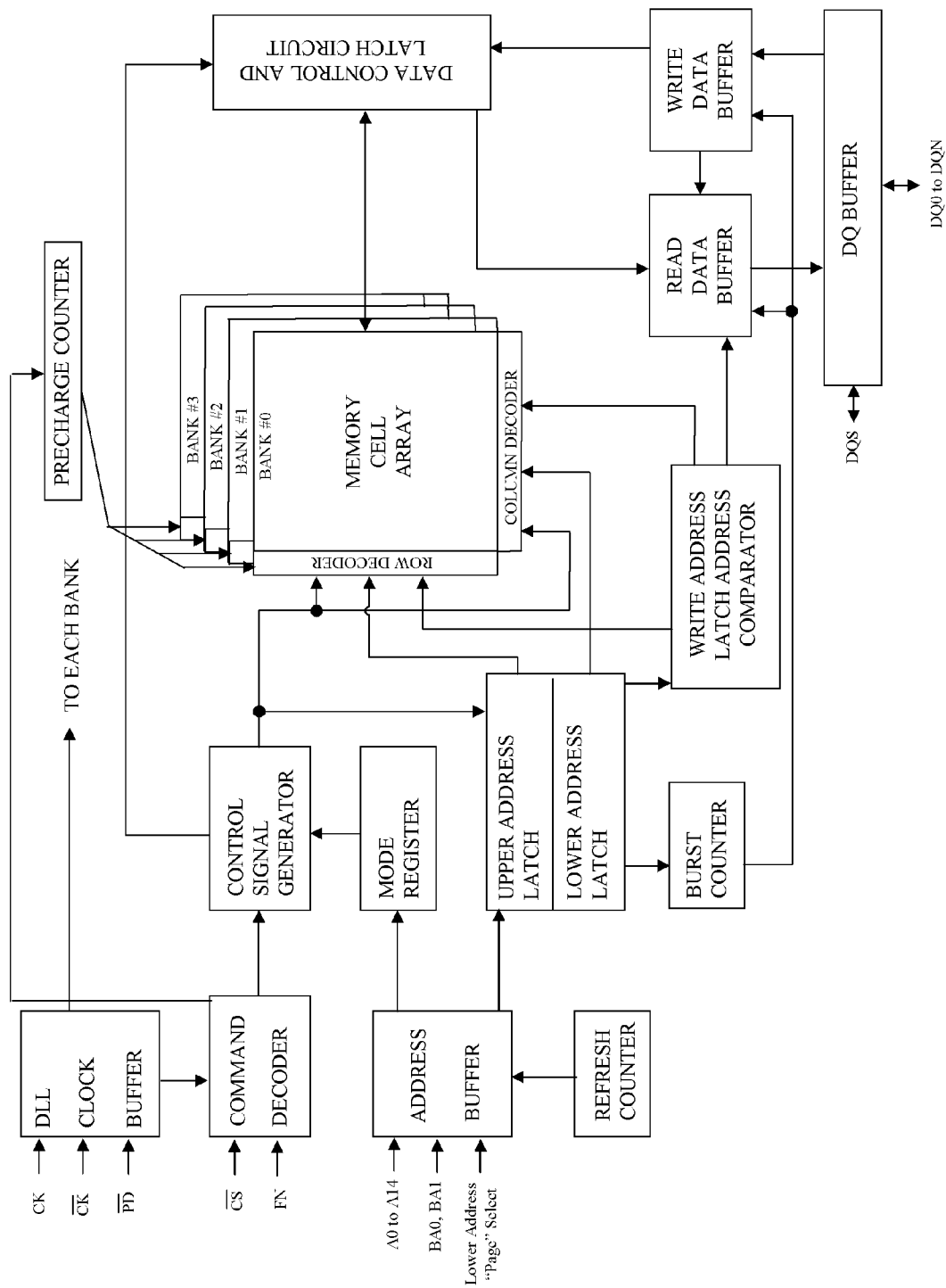
The block diagram illustrates the internal architecture of a memory device. Key components include:

- Control Logic:** Manages the overall operation, including command decoding and mode register control.
- Address Registers:** Store the row and column addresses provided by the external bus.
- Row Address MUX and Decoder:** Routes the row address to the appropriate memory array.
- Memory Array:** Consists of multiple banks (BANK 0 to BANK 3) of memory cells.
- Sense Amplifiers:** Detect the data stored in the memory array during a read operation.
- I/O Gating DM Mask Logic:** Controls the data flow between the memory array and the external data bus.
- Column Decoder:** Routes the data from the memory array to the appropriate output line.
- Column Address Counter/Latch:** Manages the column address for the column decoder.
- Read and Write Paths:** Detail the flow of data during read and write operations, including the use of input registers, write FIFOs, and output registers.
- Refresh Counter:** Manages the refresh of the memory array.
- Precharge Counter:** Manages the precharge of the memory array.
- Bank Control Logic:** Manages the operation of the individual memory banks.
- Bank Memory Array:** The core storage element, organized into banks.
- Bank Row Address Latch & Decoder:** Manages the row address for each bank.
- Bank Control L Logic:** Manages the control logic for each bank.
- Bank Memory Array (8,192 x 512 x 32):** The specific memory array configuration.
- Bank Row Address Latch & Decoder (8,192):** The specific row address management for each bank.
- Bank Control L Logic (8,192):** The specific control logic for each bank.
- Bank Memory Array (8,192 x 512 x 32):** The specific memory array configuration.
- Bank Row Address Latch & Decoder (8,192):** The specific row address management for each bank.
- Bank Control L Logic (8,192):** The specific control logic for each bank.

The diagram illustrates the internal architecture of a memory device, organized into several main functional blocks:

- Control and Addressing:** Includes **CONTROL LOGIC** (with **COMMAND DECODE** and **MODE REGISTERS**), an **ADDRESS REGISTER** (receiving A0-A12, BAO, BAI), a **REFRESH COUNTER**, and a **PRECHARGE COUNTER**.
- Row and Column Decoding:** Features a **ROW-ADDRESS MUX**, a **BANK0 ROW-ADDRESS LATCH & DECODER**, a **BANK CONTROL LOGIC**, and a **COLUMN-ADDRESS COUNTER/LATCH**.
- Memory Banks:** Consists of multiple **BANK** units (BANK 0 to BANK 3), each containing a **MEMORY ARRAY (8,192 x 512 x 32)**.
- Sense Amplifiers and I/O:** Includes **SENSE AMPLIFIERS**, **I/O GATING DM MASK LOGIC**, and **DM MASK LOGIC** connected to the memory arrays.
- Data Path and Buffers:** Features **DATA** buses, **READ LATCH**, **WRITE FIFO & DRIVERS**, **INPUT REGISTERS**, and **RCVRS** (receiving elements).
- Timing and Control Signals:** Shows various control signals like **CK, CK#**, **DQS, DQS#**, **RDQS**, **DM**, and **ODT** connected to the device's pins.

FIGURE 10



Burst Read with Auto Precharge (JEDEC Standard DDR2 DRAM Specification, September 2003)

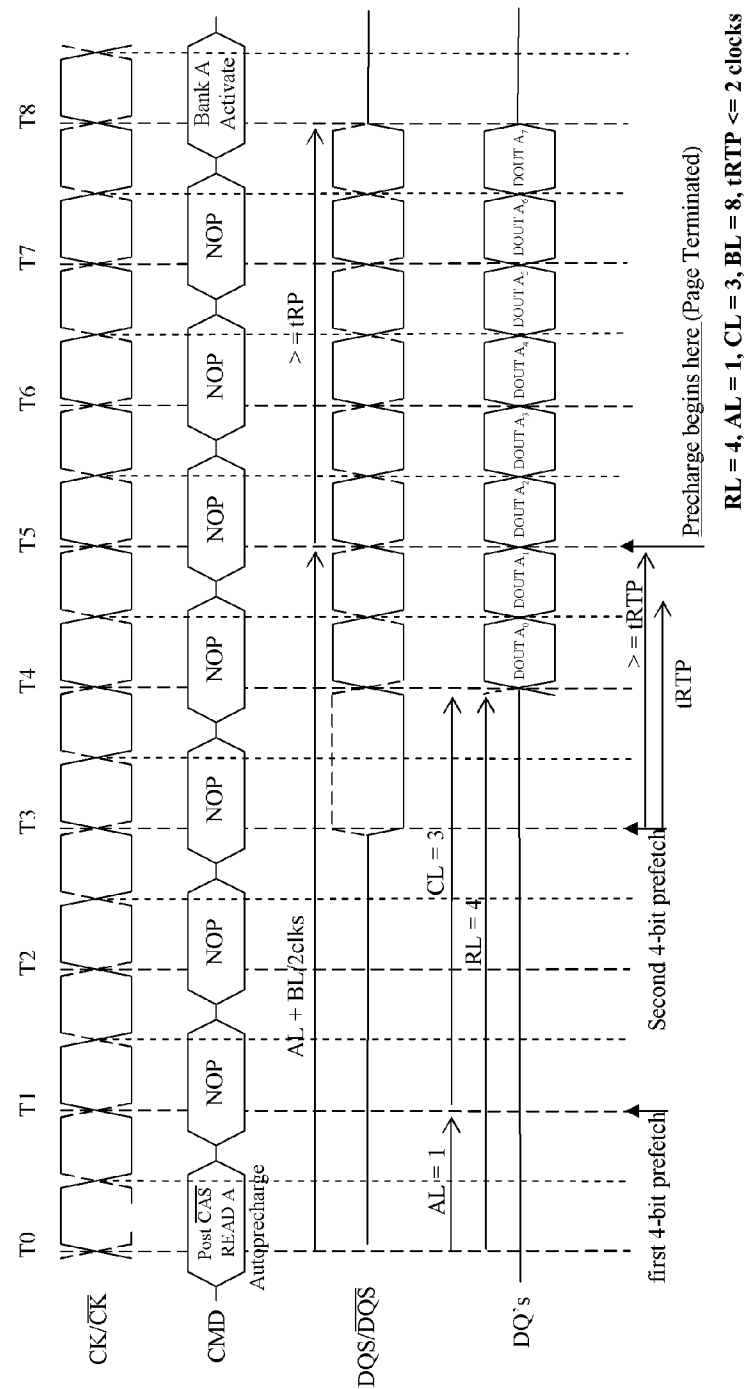
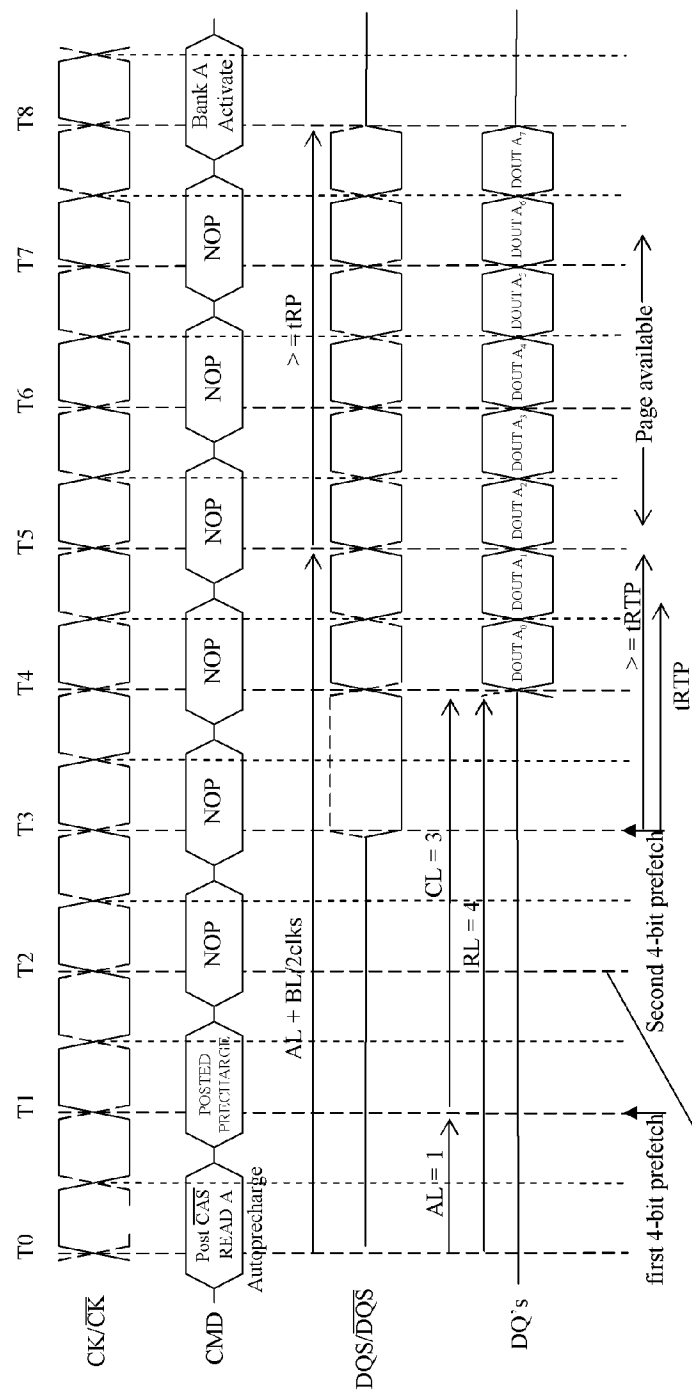


FIGURE 11

Burst Read with Posted Precharge



RL = 4, AL = 1, CL = 3, BL = 8, tRTP ≤ 2 clocks

Internal Precharge (Programmable) enable activated

FIGURE 12

